## Remarks

Claims 1-4 have been rejected under 35 U.S.C. §102(e) as being anticipated by Cho (US 6,158,039). This rejection is respectfully traversed for the following reasons.

Claim 1 is patentable over Cho, since claim 1 recites a signal processor including, in part, an error correction block operable to subject data, which has been stored in a first memory, to error correction for each predetermined error correction block; a second memory; a descrambling/error detection block operable to read the data after the error correction from the first memory, descramble the data which has been subjected to the error correction, detect errors in the data after the descrambling, and thereafter store the data in the second memory; and a controller operable to transmit error-free data which has been stored in the second memory to a host computer when the descrambling/error detection block judges that there is no error in the data which has been stored in the second memory. Cho fails to disclose or suggest a second memory as recited in claim 1.

Cho discloses a system decoder 18 having an ECC memory controller 108, a third memory 130, a fourth memory 140, an error corrector 110 and a descrambler and error detector 112. The ECC memory controller 108 receives demodulated data from an EMF demodulator 100. The system decoder 18 operates such that the controller 108 writes one correcting block of the received demodulated data into the third memory 130 in a first step. In the next step, the error corrector 110 error-corrects the data written in the third memory 130 and the controller 108 writes the next one correcting block of the received demodulated data into the fourth memory 140. In the next step, the error corrector 110 error-corrects the data written in the fourth memory 140, and the controller 108 simultaneously outputs the error-corrected data from the third memory 130 to the descrambler and error detector 112 and inputs the next one correcting block of the received demodulated data to the fourth memory 140. In the next step, the error corrector 110 error-corrects the data written in the third memory 130, and the controller 108 simultaneously outputs the error-corrected data from the fourth memory 140 to the descrambler and error detector 112 and inputs the next one correcting block of the demodulated data to the fourth memory 140. The above process is repeated until the demodulated data is no longer received from the EMF demodulator 100. (See column 3, lines 34-43; column 4, line 38 - column 5, line 21; and Figures 3 and 4).

Based on the above discussion, it is apparent that the third memory 130 and the fourth memory 140 are operable to alternatively receive correcting blocks form the controller 108 and once the correcting blocks are error corrected by the error corrector 110, the error-corrected data is alternatively output from the third memory 130 and the fourth memory 140 to the descrambler and error detector 112 to make room for the following correcting blocks. In other words, the third memory 130 and the fourth memory 140 store the correcting blocks both before and after they are corrected by the error corrector 110. On the other hand, the present invention as claimed in claim 1 recites a second memory that has data stored therein after the data passes through a descrambling/error detection block which reads the data after error correction from a first memory, descrambles the data which has been subject to the error correction, and thereafter stores the data in the second memory. It is apparent that neither the third memory 130 nor the fourth memory 140 store data after the data passes through the descrambler and error detector 112. As a result, Cho fails to disclose or suggest the present invention as recited in claim 1.

Because of the above-mentioned distinctions, it is believed clear that claims 1-4 are not anticipated by Cho. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to modify Cho or to make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claims 1-4. Therefore, it is submitted that claims 1-4 are clearly allowable over the prior art of record.

In view of the above amendments and remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be resolved before allowance of the application.

Respectfully submitted,

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